IN THE CLAIMS:

Please cancel claims 21, 22, 25 and 27 without prejudice, and amend the claims as follows:

1. (Currently Amended) A method for adjusting a level of a voltage at an output node, the voltage being generated internally to an integrated circuit device, the method comprising:

providing a voltage dividing circuit with a plurality of serially connected resistors;

supplying the voltage dividing circuit with a reference voltage, resulting in a different voltage level at nodes of the voltage dividing circuit formed between the serially connected resistors;

providing a plurality of switches, each switch configured to selectively couple the output node to a single node of the voltage dividing circuit;

providing control signals to close a single one of the switches at any given time, wherein each of the control signals corresponds to a different one of the switches and only one of the control signals is asserted at any time to close a single switch; and

generating the control signals as a function of states of one or more non-volatile storage elements, wherein the states are determined based on an output of a voltage comparator comparing the voltage at the output node to [[the]] an external reference voltage.

2-4. (Canceled)

5. (Previously Presented) The method of claim 1, wherein the non-volatile storage elements are fewer in number than the control signals.

6. (Original) The method of claim 1, further comprising providing one or more switches in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors.

7 (Currently Amended) A trimming circuit for use in adjusting a voltage at an output node, the voltage being generated internally to an integrated circuit device, comprising:

a plurality of switches, each switch configured to selectively couple the output node to a single one of a plurality of nodes of a voltage dividing circuit, wherein each node is at a different voltage level;

wherein a single switch is coupled between the output node and each node of the voltage dividing circuit; and

wherein the plurality of switches open and close in response to control signals generated as a function of states of one or more non-volatile storage elements, wherein the states are determined based on an output of a voltage comparator comparing the voltage at the output node to [[the]] an external reference voltage.

8-9. (Canceled)

10. (Previously Presented) The trimming circuit of claim 7, further comprising a decoder configured to assert a single one of the control signals as a function of the states of the one or more non-volatile storage elements.

11. (Previously Presented) The trimming circuit of claim 7, wherein the number of switches is greater than the number of non-volatile storage elements.

12. (Original) The trimming circuit of claim 7, wherein:

the voltage divider circuit comprises a number of serially connected resistors; and

the trimming circuit further comprises at least one additional switch connected in parallel to, and to selectively bypass, one of the serially connected resistors.

13. (Currently Amended) A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

a voltage generating circuit comprising a voltage divider circuit with a plurality of nodes, each at different voltage levels dependent on a reference voltage;

a plurality of switches, each switch configured to selectively couple an output node of the voltage generating circuit with a single one of the voltage divider circuit nodes; and

a plurality of non-volatile memory elements, wherein the switches are controlled by control signals generated as a function of states of the non-volatile storage elements, wherein the states are determined based on an output of a voltage comparator comparing the voltage at the output node to [[the]] an external reference voltage.

14. (Canceled)

15. (Previously Presented) The memory device of claim 13, further comprising a decoder to generate the control signals, wherein the number of control signals is greater than the number of non-volatile storage elements.

16. (Original) The memory device of claim 13, wherein the voltage generating circuit is configured to generate a negative voltage, with respect to a ground reference.

17. (Original) The memory device of claim 16, wherein the memory device is a dynamic random access memory device and the negative voltage is to be supplied to substrates of transistors of the memory cells.

18. (Previously Presented) The memory device of claim 13, wherein the memory device is a dynamic random access memory device and the voltage generating circuit is configured to generate a voltage to be supplied to wordlines of the memory cells via the peripheral circuitry.

19. (Previously Presented) The memory device of claim 13, wherein:

the voltage dividing circuit comprises serially connected resistive elements; and

the memory device further comprises at least one additional switch to selectively bypass one or more of the serially connected resistive elements.

20. (Previously Presented) The memory device of claim 19, further comprising a plurality of fuses, wherein:

a first one or more signals generated based on a first one or more of the fuses control the plurality of switches; and

a second one or more signals generated based on a second one or more of the fuses control the at least one additional switch.

21. (Canceled) A method for adjusting a level of a voltage at an output node, the voltage being generated internally to an integrated circuit device, the method comprising:

providing a voltage dividing circuit with a plurality of serially connected resistors;

supplying the voltage dividing circuit with a reference voltage, resulting in a different voltage level at nodes of the voltage dividing circuit formed between the serially connected resistors;

providing a plurality of switches, each switch configured to selectively couple the output node to a single node of the voltage dividing circuit; and

providing one or more switches in parallel with one or more of the resistors of the voltage dividing circuit, each to selectively bypass the one or more resistors.

22. (Canceled) A trimming circuit for use in adjusting a voltage generated internally to an integrated circuit device, comprising:

a plurality of switches, each switch configured to selectively couple an output node on which the voltage is supplied to a single one of a plurality of nodes of a voltage dividing circuit, wherein each node is at a different voltage level;

wherein the voltage divider circuit comprises a number of serially connected resistors; and

wherein the trimming circuit further comprises at least one additional switch connected in parallel to, and to selectively bypass, one of the serially connected resistors.

23. (Canceled)

24. (Canceled)

25. (Canceled) A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

a voltage generating circuit comprising a voltage divider circuit with a plurality of nodes, each at different voltage levels dependent on a reference voltage; and

a plurality of switches, each switch configured to selectively couple an output node of the voltage generating circuit with a single one of the voltage divider circuit nodes,

wherein the voltage dividing circuit comprises serially connected resistive elements; and

wherein the memory device further comprises at least one additional switch to selectively bypass one or more of the serially connected resistive elements.

26. (Currently Amended) ~~The memory device of claim 25, wherein:~~ A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

a voltage generating circuit comprising a voltage divider circuit with a plurality of nodes, each at different voltage levels dependent on a reference voltage; and

a plurality of switches, each switch configured to selectively couple an output node of the voltage generating circuit with a single one of the voltage divider circuit nodes,

wherein the voltage dividing circuit comprises serially connected resistive elements;

wherein the memory device further comprises at least one additional switch to selectively bypass one or more of the serially connected resistive elements;

wherein a first one or more signals generated based on a first one or more of the fuses control the plurality of switches; and

wherein a second one or more signals generated based on a second one or more of the fuses control the at least one additional switch.

27. (Canceled) A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

a voltage generating circuit comprising a voltage divider circuit with a plurality of nodes, each at different voltage levels dependent on a reference voltage, wherein the voltage dividing circuit comprises serially connected resistive elements;

a plurality of switches to selectively couple an output node of the voltage generating circuit with a single one of the voltage divider circuit nodes;

at least one additional switch to selectively bypass one or more of the serially connected resistive elements; and

a plurality of non-volatile memory elements, wherein the switches are controlled by control signals generated based on states of the non-volatile storage elements.

28. (Currently Amended) A memory device comprising:

peripheral circuitry;

a plurality of memory cells;

a voltage generating circuit comprising a voltage divider circuit with a plurality of nodes, each at different voltage levels dependent on a reference voltage, wherein the voltage dividing circuit comprises serially connected resistive elements;

a plurality of switches to selectively couple an output node of the voltage generating circuit with a single one of the voltage divider circuit nodes;

at least one additional switch to selectively bypass one or more of the serially connected resistive elements;

a plurality of non-volatile memory elements, wherein the switches are controlled by control signals generated based on states of the non-volatile storage elements; and

~~The memory device of claim 27, further comprising a~~ plurality of fuses, wherein:

a first one or more signals generated based on a first one or more of the fuses control the plurality of switches; and

a second one or more signals generated based on a second one or more of the fuses control the at least one additional switch.